DETAILED ACTION

Election/Restrictions

Applicant's election of Group II (claims 4-12) in the reply filed on 3/2/2010 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

1. Claims 1-3 and 13-15 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected subject matter.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 4, 5, 6, 7, 8, 9, 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kazuto (JP2002-76185) in view of Citation 2 (JP H07-283280).

Regarding claim 4 – Kazuto teaches a method of manufacturing a wiring board member for forming a multilayer wiring board, comprising: a step of forming a mask ([paragraph 0035] Kazuto states, "a thermal oxidation film is first formed on the silicon") having a certain opening pattern ([paragraph 0035] Kazuto states, "the square opening") on a surface of a silicon substrate (50) whose main surface is (100) face ([paragraph 0035]

Kazuto states, "the silicon single crystal wafer of p type (100) plane direction"); a step of forming a recess (51) of a substantially quadrangular pyramid shape ([paragraph 0036] Kazuto states, "a reverse pyramid") or a substantially truncated quadrangular pyramid shape on a surface of the silicon substrate (see fig. 2a), by a crystal anisotropy etching ([paragraph 0035] Kazuto states, "anisotropic etching as shown in formation of the crevice 51") of the silicon substrate through the mask with a chemical liquid ([paragraph 0036] Kazuto states, "Then, a silicon oxide film is etched with fluoridation ammonium and fluoric acid mixed solutions, and silicon is exposed"; These are chemical liquid etchants); a step of removing the mask from the surface of the silicon substrate (see fig. 2a);

a step of forming an insulation layer (fig. 2f, 31) on the surface of the silicon substrate; a step of forming a conductive layer (fig. 2e, 32) on the surface of the silicon substrate on which the insulation layer have been formed (see fig. 2f), the conductive layer occupying the recess (see figure 2g); and a step of separating (see fig. 2g to fig. 2h) the insulation layer (31) and the conductive layer from the silicon substrate to obtain a wiring board member (fig. 1, 30) including the insulation layer and the conductive layer

Kazuto does not teach wherein forming the insulation layer on the surface of silicon other than a part where the recess is formed; and wherein the conductive layer covers the insulation layer.

Citation 2 teaches a method of manufacturing a wiring circuit board (fig. 1a, 100) wherein forming the insulation layer (fig. 1f, 32) on the surface of silicon (26) other than

a part where the recess is formed (see figure 1f); and wherein the conductive layer (fig. 1h, 36) covers the insulation layer.

It would have been obvious to a person having ordinary skill in the art at the time of invention to modify the method of manufacturing a wiring circuit board taught by Kazuto with the specific areas covered by the insulator and the conductive layer covering the insulation because both of these steps will increase the conductivity of the contact terminals, and therefore create a more reliable terminal.

Regarding claim 5 – Kazuto in view of Citation 2 further teach a method of manufacturing a wiring board member further comprising, between the step of removing the mask (Kazuto; fig. 2a; Discussed in the rejection to claim 1) and the step of forming the insulation layer (fig. 2f, 31), a step of forming a separation layer (fig. 2b, 52) on the surface of the silicon substrate for facilitating separation of the insulation layer and the conductive layer from the silicon substrate.

Regarding claim 6 – Kazuto teaches a method of manufacturing a wiring board member wherein the step of separating the insulation layer (fig. 2g, 31) and the conductive layer (fig. 2e, 32) from the silicon substrate (50) is conducted by an exfoliation process ([paragraph 0051] Kazuto states, "the template 50 exfoliates from an interface with the seed layer 52").

Kazuto alone does not teach dissolving a layer by a process liquid.

Citation 2 teaches a method of manufacturing a wiring board member (fig. 1) wherein a layer (fig, 1b, 27) is dissolved by a process liquid ([paragraph 0061] Citation 2 states, "the 2 oxidization silicone film 27 exposed by the opening 29 is immersed in 1:7 of hydrofluoric acid and ammonium fluoride liquid, and is etched").

It would have been obvious to a person having ordinary skill in the art at the time of invention to modify the method of manufacturing a wiring board member taught by Kazuto with the liquid process taught by Citation 2 because using a process liquid is a fast and economical way to remove unwanted material from a wafer.

Regarding claim 7 – Kazuto in view of Citation 2 further teach a method of manufacturing a wiring board further comprising a step of forming a certain wiring pattern ([paragraph 0038] Kazuto states, "the wiring 32 is formed by the pattern plating method") in the conductive layer (fig. 2e, 32).

Regarding claim 8 – Kazuto in view of Citation 2 teach a method of manufacturing a wiring board wherein the mask (Citation 2, fig. 1b, 28) is formed of a metal film ([paragraph 0067] Citation 2 states, "the mask of the above-mentioned aluminum").

Regarding claim 9 – Kazuto in view of Citation 2 further teach a method of manufacturing a wiring board member wherein the mask (Discussed in the rejection to claim 1) is formed of a silicon oxide film ([paragraph 0036] Kazuto states, "a silicon oxide film).

Regarding claim 11 – Kazuto in view of Citation 2 further teach a method of manufacturing a wiring board member wherein the insulation film (Kazuto; fig. 2c, 53) is a resist film ([paragraph 0038] Kazuto states, "resist film 53").

Regarding claim 12 – Kazuto in view of Citation 2 teach a method of manufacturing a wiring board member wherein the step of forming the conductive layer (Citation 2; fig. 1i, 39) is conducted by a plating with copper ([paragraph 0071] Citation 2 states, "plating film 39 of copper") or copper alloy.

4. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kazuto in view of Citation 2 as applied to claim 4 above, and further in view of Gonzalez et al. (US PG. Pub. 2003/0190766 A).

Regarding claim 10 – Kazuto in view of Citation 2 teach the method of manufacturing a wiring board member according to claim 4, but fail to teach wherein the chemical liquid is selected from the group consisting of a potassium hydroxide solution, an ethylenediamine pyrocatechol solution, and a tetramethyl ammonium hydroxide solution.

Gonzalez teaches a method of manufacturing a wiring board member wherein the chemical liquid is selected from the group consisting of a potassium hydroxide solution, an ethylenediamine pyrocatechol solution, and a tetramethyl ammonium

hydroxide solution ([paragraph 0047] Gonzalez states, "the etch recipe is a wet tetramethyl ammonium hydroxide (TMAH) etch").

It would have been obvious to a person having ordinary skill in the art at the time of invention to modify the method of manufacturing a wiring board member taught by Kazuto in view of Citation 2 with the specific etching chemical taught by Gonzalez because Gonzalez states, "The TMAH etch chemistry is desirable because it is selective such that it etches the bulk silicon of the substrate 10, but does not substantially etch the nitride film 24" [paragraph 0047].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVEN SAWYER whose telephone number is (571)270-5469. The examiner can normally be reached on Mon-Thu 7:00-5:30 (est).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jinhee Lee can be reached on 5712721977. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ishwarbhai B Patel/
Primary Examiner, Art Unit 2841

/S. S./
Examiner, Art Unit 2841